Industry Specificities: Technology and Innovation Capabilities of Semiconductor Foundries

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1. Introduction

Evolutionary economists have strived to examine the mechanisms behind the rapid economic development of what began as very backward countries in East Asia. South Korea and Taiwan are two major examples of how latecomer countries can catch-up with the forerunners through rapid technological upgrading. Gerschenkron (1962) pioneered the 'latecomer effect' in his search to explain the latecomer economic development in the 19th century among European countries. According to Gerschenkron (1962), the more technologically backward a country is, the shorter period it requires to catch-up with the forerunners. The speed of catch up is therefore very much dependent on locations, industry type and the timing of pursuit (Rasiah and Vinanchiarachi, 2012).

Although the fact that technology as a factor of economic growth was generally acknowledged by the neo-classical economists since the early 20th century, evolutionary economists believe that economic growth cannot be understood as an undifferentiated, aggregate phenomenon, but rather it is determined by the country's different sectors, each characterized by its own dynamics (Nelson, 2008). Industry specificities appropriately shape and condition the institutions and institutional change essential to drive technological upgrading (Nelson, 2008; Rasiah and Vinanchiarachi, 2012). Motivated by the importance of understanding such specificities, the objective of this paper is to examine the evolutionary argument that technological upgrading is industry specific by researching inductively the technological capabilities of firms from Taiwan, South Korea and Malaysia in the semiconductor foundry industry.

Adapting from the technological taxonomy and trajectory developed by Rasiah (2010), this paper attempts to map a technology typology specifically for the semiconductor foundries. This paper argues that technological capability building is industry specific; and that the dynamic model of process and product innovation of Utterback and Abernathy (1975) remains relevant to a certain extent and in fact is influenced by the technological regime of the industry, i.e. Schumpeterian patterns of innovation. The rest of the paper is organized as follows. Section 2 discusses the theoretical considerations pertaining to the development of

the technological taxonomy and trajectory of semiconductor foundries. Section 3 presents the proposed typology and explains the rationale behind whereas section 4 analyzes the empirical evidence. Section 5 concludes.

2. Theoretical Considerations

This paper takes the direction of 'appreciative theorizing', which explores industry specificities, dynamics of competition and the basics of what is actually going on (Nelson and Winter, 1982; Nelson, 2008b: 20). Each technology and knowledge intensive industry is especially governed and conditioned by its own specificity, tacitness, complexity and independence when compared to another industry (Winter, 1987). Therefore, the evolutionary approach to understanding technology requires that different industries are studied uniquely in order to comprehend the underlying dynamics that change with time and space (Rasiah and Vinanchiarachi, 2012).

The conceptual basis for the typology of semiconductor foundries proposed in this paper rests on the linkages between two main theories of technology development. First, the typology seeks to demonstrate that firm-level technological capability building is conditioned by Schumpeterian patterns of innovation, i.e. Schumpeter Mark I and Mark II, of which Malerba and Orsenigo (1996) referred as the 'widening' pattern and the 'deepening' pattern respectively.[1] Second, the typology reorganized the importance of understanding the relationship between process and product development as argued in the dynamic model of innovation by Utterback and Abernathy (1975), and that this relationship is affected by Schumpeterian patterns of innovation.

2.1 Schumpeterian patterns of innovation

The semiconductor foundry industry offers a unique example to demonstrate Schumpeterian patterns of innovation. The industry is characterized by Schumpeter Mark I (creative destruction) features in its beginning stage. Schumpeter Mark I activities refer to innovations that rely on existing stocks of knowledge (Schumpeter, 1912). Firms underpinned by the

[1] The pattern of innovation (Schumpeter Mark I or II) is dependent on the industry's technological regime. Technological regime can be understood as the nature of technology representing a set of knowledge environment that allows firms to conduct problem-solving activities (Winter, 1984: p.289). It can also be referred to as the attributes that mould the development of physical technologies in a particular industry (Nelson, 2008a). To understand Schumpeterian patterns of innovation from the perspective of technological regime, see Malerba and Orsenigo (1996) and Breschi et al (2000).

Mark I innovation pattern either combine different types of knowledge or adapt existing stocks of knowledge to deliver new processes, incremental or minor innovations of products and change of organizational structures (Rasiah, 2010).

Firms in the industry that progress through the life cycle and reach the technology frontier will transit to Schumpeter Mark II (creative accumulation).[2] While Schumpeter (1934) had argued that entrepreneurs are the key players to trigger small technical changes through creative destruction, he (1943) considered the modern firm and those able to invest heavily in R&D as the key drivers of radical technological changes. Schumpeter (1943:84) had argued that entrepreneurs are typically too small and lack the critical mass of capital to undertake frontier technology research unless external support is given. Several requirements are essential for established firms in a Schumpeter Mark II industry to launch new streams of knowledge, including accumulation of knowledge stocks, R&D competence, production and distribution, and sufficient financial resources (Breschi et al., 2000).[3]

Moreover, the semiconductor industry requires creative accumulation because of the cumulative nature of technical advances in the knowledge regime, which means that the technological innovation of the future is the result of present efforts to reduce the minimum linewidth in chip implants. The semiconductor industry is a knowledge and technology intensive industry. It is unique as the industry's technological development has been governed by Moore's Law since the introduction of the theory by the co-founder of Intel in 1965. Moore's Law says that transistor density in ICs doubles while the minimum linewidth halves approximately every two years (Dubash, 2005). In Dynamic Random Access Memories (DRAM), Hwang's law has quickened this process to every one year (see Rasiah et al., 2012). Since then, the laws have been the firms' long term technology plans and R&D targets[4] whereas firms which are not able to keep up with the incessant miniaturization retreat to product innovations at existing nodes.

[2] Evolutionary economists have posited the possibility of a firm switching its strategy from Schumpeterian Mark I to Schumpeterian Mark II (Breschi et al., 2000).

[3] Firms operating under the Schumpeterian Mark II environment is characterized by low opportunities, appropriability and cumulativeness with strong internalized tacit and explicit knowledge base which cause a "high degree of concentration of innovative activities, low rates of entry and remarkable stability in the hierarchy of innovators" (Breschi et al, 2000: 395).

[4] Latecomers can determine a catch-up roadmap for themselves. It is analogous to the relative speed of runners racing on a path set by forerunners (Perez, 1988: p.86).

2.2 Utterback and Abernathy's (1975) dynamic model of innovation

As Abernathy and Utterback (1975: p.640) had argued, there is a strong interdependent relationship between a firm's strategy and its environment and that a chosen strategy leads to interactions between the types of process and product innovation that a firm undertakes and the way its productive resources are deployed. One of the top challenges for competitive firms is the management of the product-process connection (Ettlie, 1995, p.1224).

Patterns of industrial innovations can be explained as following three generic phases, namely Fluid Phase, Transitional Phase and Specific Phase, which identify and separate process and product innovation (Abernathy and Utterback, 1978). The rate of process or product innovation is argued to be dependent on the particular phase the industry or the product is in.[5] The industry devotes most attention to product innovation or product varieties rather than process innovation in the first phase. The reverse happens in the second phase where producers search for 'dominant designs' which enables them to proceed to standardized manufacturing later. The Specific Phase is the period which firms divert from both process and product innovations, but strive toward competitiveness in terms of cost, volume and capacity.

It is common for researchers to analyze the catch-up experience of latecomers by identifying certain general patterns. Extended from Utterback and Abernathy's (1975) dynamic model of process and product innovation, Kim (1980, 1997) presented another three-stage technology development model to show that firms go through acquisition, assimilation and improvement of foreign technologies. According to Kim (1997, 1999), developing countries reverse the direction of technological trajectory in advanced countries as proposed by Utterback and Abernathy. Therefore, when successful NIEs like South Korea and Taiwan arrive at the emerging technology stage (for innovation), it is equivalent to the "Fluid" stage in Abernathy and Utterback's (1978) notion (see Kim, 1999, p. 114).[6]

This "Fluid" stage is also known as the stage of "systemic process" (Utterback and Abernathy, 1978). At this stage, firms' production system is further standardized while cost

[5] This model can be applicable to the life cycle of a single product line, a manufacturing process, a specific product generation and the growth of an entire industrial branch related to a product generation.

[6] In Kim's notion, firms evolve from mature technology stage to the intermediate technology stage and finally to the emerging technology stage. The technological trajectory of the model can also be recognized as 'duplicative imitation', 'creative imitation' and lastly 'innovation' (Kim 1997).

minimization is the ultimate important goal. A tighter relationship between process and product features occurs at this juncture and that the two are considered highly interdependent by the managers. Eventually, the probability of further radical innovations in both the product and the process system decreases as a result of the standardization process.

While the model remains relevant and insightful, there are some limitations when it comes to applying Abernathy and Utterback's model to a high-tech industry, or specifically the semiconductor foundry industry as it does not incorporate the influence of the industry's technological regime, i.e. Schumpeterian patterns of innovation in this paper. The argument made by the model on the rate of process and product innovation does not deal with specificities of the foundry industry.

2.3 Technological taxonomy and trajectory

Innovation can be defined as a successful market commercialization of a new or better product or process (Pavitt, 1984, p. 344). Innovations can be classified by their relative importance, which distinguishes radical from incremental innovations and by their object, either process or product (Perez, 1988). Generally, process technology is regarded as the processes undertaken to process or assemble products (Rasiah, 1994). It involves machinery and equipment, layouts, inventory and quality control systems, production organization and firm-structures (Rasiah, 1996). Catch up in product technology is more complex as it generally involves intellectual property rights, huge investments and sustained participation in R&D of products with shortening product cycles.

To determine the level of knowledge accumulation or technological capabilities of firms, different typologies that document firm-level learning trajectories have been introduced. Different variables of technological capabilities can be understood by classifying them into a framework with specific technological taxonomy and trajectories. Technological trajectories can be referred as the directions of technical development which are cumulative and internally self-generating (Dosi, 1982: p.154). It can also be defined as the pattern of progress, i.e. of "normal" problem solving activity on a ground of a technological regime (Dosi, 1982, p.152). It is a cluster of possible technological directions whereby the nature of the regime defines its boundaries.

As Utterback and Abernathy (1975) have emphasized the significance to examine firms' 'rate' of innovation, it is clearly essential for a technological typology to be able to capture

the time required or rather the speed of technological development. Lee (2005) argued that the speed of technological upgrading varies among latecomers, with some catching up successfully while others remain as technology laggards. The speed at which a firm builds its technological capabilities also affects the types of innovation the firm can undertake (Figueiredo, 2010). Nevertheless, majority of the existing frameworks of latecomers' technological capabilities have not been able to fully explain the issues of time and speed of latecomers' transition from one level to the other (Bell, 2006). Furthermore, many of the existing studies on technological and innovation capability frameworks are based on the assumption of long-term continuity in firms to accumulate capability by following certain technology trajectories and pay less attention to the possibility of discontinuity (Figueiredo, 2010).

Since East Asian industrialization has been significantly driven by manufacturing sectors, studies on East Asian firm-level accumulated capabilities have been mostly focused on the technological taxonomy and trajectory founded on assembled and discrete product manufacturing (Figueiredo, 2010). Firms are generally assessed based on their ability to progress from assembly and test to minor development, improved development and eventually product designing capabilities (Lee and Lim, 2001). These frameworks however are not specific enough to examine technological capabilities of firms in high tech industries such as the semiconductor foundry industry.

The direction and dynamics of technological capability building in semiconductor foundries are not fully understood. This paper takes one step further to scrutinize the technological taxonomy and trajectory of semiconductor foundries by incorporating the areas outlined above which have previously received less attention. A more systematic and industry-specific firm-level scrutiny will enhance our understanding of firm's technology bottlenecks thus provide insights to firms' strategic management as well as industrial policy making.

3. Towards a Technological Typology of Semiconductor Foundries

The technological capability framework proposed in this paper is adapted and extended from Rasiah's (2010) work on firm-level technological taxonomy and trajectory. It is a typology that draws on the model initially proposed by Lall (1992) and developed further by Rasiah (2004, 2011). Whereas Rasiah's (2010) framework focused on the technological capabilities of electronics firms and represents a useful guidance to map the technological capabilities of

consumer electronics, industrial electrics and semiconductor firms, the proposed typology in this paper attempts to extend the framework by incorporating the specificities and dynamics of the foundry industry.

Table 1 shows the proposed firm-level typology by taxonomies and trajectories adapted from Rasiah (2010) to evaluate technological capabilities of semiconductor foundries. Following the convention of Rasiah (2010), the typology evaluates firms based on the depth and trajectory of knowledge which systematically rank firms into six levels. Whereas Rasiah (2010) referred levels 4 – 6 as the innovation-generating activities that require extensive R&D, the proposed typology in Table 1 seeks to elaborate on the original idea by incorporating the influence of the industry's innovation pattern, in this sense the Schumpeter Mark I and Schumpeter Mark II industry characteristics. The proposed typology makes the distinction between level 1 - 4 (Schumpeter Mark I) and level 5 - 6 (Schumpeter Mark II).

3.1 From Schumpeter Mark I to Schumpeter Mark II

Level 1 – 4 are labeled under Schumpeter Mark I because the technological capabilities of firms operating at these levels have not gone beyond creative destruction to keep up with the industry's technological evolution, in this case the increasing wafer diameters and miniaturization of process nodes are the two biggest challenges. Firms which are not able to break the mold and transit to Schumpeter Mark II activities are trapped at level 4 and their technology activities are limited to "horizontal expansion" of product features, i.e. the 'More than Moore's Law'.

As the semiconductor foundry industry evolves, firms have been constantly governed by the increasing wafer diameters and incessant miniaturization of technology nodes. The industry has arrived at a state where large firms require Schumpeterian creative accumulation strategy to stay competitive and to keep up with the radical technological changes. Large and established foundries with wafer fabrication plants impose high barriers of entry to the industry as the required costs to start production have skyrocketed in recent years. The cost of setting up a wafer fabrication plant has been increasing exponentially year-by-year since 1994, from US$ 7 million in 1994 to US$ 6 billion in 2009 (Vajpayee and Dhasmana, 2011).

Furthermore, knowledge accumulation (Mark II) becomes an integral part of foundry firms as the industry is governed by the Moore's law which requires a firm's development of a smaller technology node acts as a guidance for the firm's future development of subsequent

Table 1: Technological taxonomy and trajectory of semiconductor foundries

Schumpeterian Innovation Pattern	KNOWLEDGE DEPTH	Utterback and Abernathy Dynamic Model of Innovation													
		PROCESS				PRODUCT									
		Wafer Size Migration (mm)	Minimum Linewidth (µm)		Description	Minimum Linewidth (µm)	More than Moore (Horizontal Expansion of Product Features)								
							M1	M2	R	A	B	C	D1	D2	L
Schumpeter Mark I	Level 1 : Simple Activities	<100	MORE MOORE (RACE OF MINIATURIZATION)	>1	Dated processes with normal manufacturing techniques	>1	Processing of component using foreign technology								
	Level 2 : Minor Improvement	125		1	Advanced machinery,layouts & problem solving	1	Precision engineering								
				0.7		0.7									
				0.5		0.5									
	Level 3: Major Improvement	150		0.35	Cutting-edge manufacturing techniques	0.35	Original equipment manufacturing (OEM) capability with minimum product adaption capability								
				0.25		0.25									
				0.18		0.18									
				0.13		0.13									
	Level 4 : Engineering	200		0.09	Process adaptation: layouts, equipment & techniques	0.09	Product adaptation								
				0.065		0.065									
Schumpeter Mark II	Level 5: Early R&D	300		0.045	Process development capability	0.045	Product development capability, with some firms developing original design capability.								
				0.032		0.032									
	Level 6: Mature R&D			0.028	Advanced process R&D	0.028	New product development capability								
				0.022		0.022									
		INCREASING WAFER SIZE	SLOWING DOWN OF MOORE'S LAW												
		Continued Maximization	Continued Miniaturization			Continued Miniaturization	Advanced Integration								
		450mm	<22nm			<22nm	CoWoS (2.5D Packaging)								
							3D Packaging								

Source: Adapted from Rasiah (2010).

M1 = MEMS; M2 = MCU (Embedded Flash); R = RF CMOS; A = Analog; B = BCD - Power IC; C = CMOS Image Sensor; D1 = High Voltage Driver; D2 = Embedded DRAM; L = Logic.

nodes. Moreover, by 2011, the process development costs for 32nm technology node reaches US$ 900 million whereas the development costs for 22nm technology node was estimated to reach US$ 1.3 billion (Vajpayee and Dhasmana, 2011).

The proposed typology also incorporates the dynamics of the industry as it evolves through time. At level 6 in the typology, firms are expected to have the required technological capabilities to respond to the continued maximization of wafer size and the slowing down of Moore's Law, which has been the predefined technology path for industry frontiers. Moore's Law is approaching physical limitations and is expected to break down if new lithography solutions are not found (LaPedus, 2007; Brown and Linden, 2009). According to TSMC's founder – Morris Chang, the law will be obstructed by unsolvable technical challenges such as power leakage in the next six to eight years (Lu et al., 2012). Foundry firms at this juncture are expected to have two divergent roadmaps which can be pursued concurrently – continued node miniaturization (at a much slower and ineffective pace) or advanced integration across the value chain (such as advanced 3D packaging service). Therefore, this proposed typology also takes into consideration the possibility of discontinuity as discussed in an earlier section.

The focus of this paper is on latecomer firms in the semiconductor foundry industry, including the ones in Taiwan, South Korea and Malaysia. Following Kim's (1997, 1999) framework, frontier foundries from the two NIEs (South Korea and Taiwan) are considered to have arrived at the emerging technology stage, i.e. "Fluid" phase in Abernathy and Utterback's (1978) notion. Given the explained industry dynamics, however, it is expected that Abernathy and Utterback's argument on the rate of process and product innovation is not applicable when it comes to the specificities of the foundry industry. While their argument pertaining to the mutual relationship between process and product innovation remains highly relevant and insightful, it is expected in this paper that the process and product innovations are affected by Schumpeterian patterns of innovation as well as discontinuities of technology trajectory.

3.2 The semiconductor foundry industry

There are some additional facts regarding the foundry industry that are important to take note before proceeding to the next section which presents the empirical evidence. Unlike the conventional vertically integrated multinationals which design and manufacture their own chips with the company's brand name, i.e. the 'integrated device manufacturer' (IDM),

TSMC became the world's first 'pure-play foundry' in the semiconductor industry in 1987 as a 'dedicated' fabrication service provider for others. A foundry is a chip manufacturer which fabricates wafers for any other semiconductor firms with the customers' brand names. Since the company's inception, the entire landscape of the semiconductor industry has changed as many chip design firms (fabless) are no longer required to deploy heavy investments into building wafer fabs because they can easily outsource their chip manufacturing to the foundries. Moreover, the financial resources are directed by the fables firms to solely focus on R&D which have spiraled more aggressive innovations of the industry. By 2010, the fabless industry has grown into a US$ 73.6 billion industry (Perry, 2011). Some giant semiconductor firms have also begun to seize the market opportunities by establishing their own foundry arm, e.g. the Korean large conglomerate firm – Samsung.

As of 2010, the world first and second largest foundries based on revenues and market share are TSMC and UMC respectively from Taiwan. The world third largest foundry - Globalfoundries is owned by the Advanced Technology Investment Company (86%), an investment firm owned by the Abu Dhabi Government, as well as Advanced Micro Devices (14%) (George-Cosh, 2010). However, 5 out of 6 wafer fabs owned by Globalfoundries are bought over from a Singaporean firm called Chartered Semiconductor in 2009. SMIC of China is the world fourth largest foundry as of 2010 which makes the world top four foundries are attributed to latecomer firms. Majority of the manufacturing capacity of Samsung foundry has been 'locked in' for Apple to make A4 and A5 chips for the iPad and iPhone (Lu et al., 2012a). Therefore the industry has not considered the sales for Apple as part of Samsung foundry services since the deal was rather locked in due to the two firms' business relationship and majority of the foundry's capacity was reserved for Apple (Gartner, 2012a).

Also, it is important to note that the focus of this paper is specifically the semiconductor foundry industry and not including the DRAM industry. In order to with industry specificity, it is important to draw the distinction because the foundry and the DRAM industry face different technological trajectories. For instance, on one hand, the foundry industry is highly dependent on the race of miniaturization (also called 'More Moore' strategy) and the product trajectory relies on the horizontal expansion of technology features at the existing process nodes ('More than Moore' strategy). On the other hand, the product trajectory of DRAM industry relies on firms' capabilities to increase the memory size of the chip, e.g. from 1M to

4M, 16M, 64M, 256M, 1G and so on. Therefore the proposed typology in this paper specifically considers the technological taxonomy and trajectory of the foundry industry, not the DRAM industry.

The proposed typology forms the 'More than Moore' trajectory on the basis of the strategy outlined by the largest foundry in the industry – TSMC. One of the company's corporate product strategies is the so-called 'MR. ABCD'. MR. ABCD is a range of products and technology features which TSMC expands horizontally at each process node, they are M1 – MEMS, M2 – MCU (Embedded Flash), R - RF CMOS, A – Analog, B – BCD Power IC, C – CMOS Image Sensor, D1 – High Voltage Driver, D2 – Embedded DRAM, and the core foundry product, L – Logic. As Moore's Law slows down (discontinuity of a technology trajectory), frontier players of the industry began to seek possibilities to strengthen their industry leadership. TSMC (foundry) and Xilinx (fabless) began serious R&D in an advanced packaging technology - Chip on Wafer on Substrate (CoWoS), of which will allow them to continue dominate the industry by achieving significant cost savings as well as improved performance.[7] Some other important technological aspects include the migration to bigger wafer size, which is a critical path for manufacturers to move towards cost minimization.

4. Result and Analysis

Six semiconductor foundries are selected in this study: the world top four pure-play foundries - Taiwan Semiconductor Manufacturing Company (TSMC) and United Microelectronics Corporation (UMC) from Taiwan, Globalfoundries owned by the state government of UAE, Semiconductor Manufacturing International Corporation (SMIC) from China; the largest foundry from South Korea – Samsung; and the one and only Malaysian owned pure-play foundry - Silterra. The technological capabilities of the six firms are assessed and graded according to their level of knowledge depth in the proposed typology. Empirical data are gathered from reliable sources such as Gartner, Credit Suisse Research, company official webpages and reports. Table 2 presents the scoring results for the six foundries.

[7] CoWoS allows wafer level packaging and silicon interposer between chip and substrate, of which system performance will be significantly improved while board space is optimized. Subsequently smaller dies lead to less defected dies, which greatly improves yield. Other positive results include flexible design, shorter time-to-market and better heat dissipation (Lu et al., 2012a).

Table 2: Technological capabilities of six semiconductor foundries

Schumpeter Innovation Pattern	KNOWLEDGE DEPTH	Utterback and Abernathy Dynamic Model of Innovation														
		PROCESS					PRODUCT									
		Wafer Size Migration (mm)		Minimum Linewidth (μm)			Minimum Linewidth (μm)	More than Moore's (Horizontal Expansion of Product Features)								
								M1	M2	R	A	B	C	D1	D2	L
Schumpeter Mark I	Level 1 : Simple Activities	<100	a,b,c,d,e,f	MORE MOORE (RACE OF MINIATURIZATION)	>1	a,b,c,d,e,f	>1	a	a	a,b,c,f	a,d,e,f	a,d	a	a,c,f	a,d	a,b,c,d,e,f
	Level 2 : Minor Improvement	125	a,b,c,d,e,f		1	a,b,c,d,e,f	1	a	a	a,b,c,f	a,d,e,f	a,d	a	a,c,f	a,d	a,b,c,d,e,f
					0.7	a,b,c,d,e,f	0.7	a	a	a,b,c,f	a,d,e,f	a,d	a	a,c,f	a,d	a,b,c,d,e,f
					0.5	a,b,c,d,e,f	0.5	a	a	a,b,c,f	a,d,e,f	a,d	a	a,c,f	a,d	a,b,c,d,e,f
	Level 3: Major Improvement	150	a,b,c,d,e,f		0.35	a,b,c,d,e,f	0.35	a	a	a,b,c,f	a,d,e,f	a,d	a	a,c,f	a,d	a,b,c,d,e,f
					0.25	a,b,c,d,e,f	0.25	a	a	a,b,c,f	a,d,e,f	a,d	a	a,c,f	a,d	a,b,c,d,e,f
					0.18	a,b,c,d,e,f	0.18	a	a	a,b,c,f	a,d,e,f	a,d	a	a,c,f	a,d	a,b,c,d,e,f
					0.13	a,b,c,d,e,f	0.13	a	a	a,b,c,f	a,d,e	a	a	a,c,f	a,d	a,b,c,d,e,f
	Level 4 : Engineering	200	a,b,c,d,e,f		0.09	a,b,c,d,e	0.09		a	a,b.c	a,d,e		a	a	a,d	a,b,c,d,e
					0.065	a,b,c,d,e	0.065			a,b.c	a				a,d	a,b,c,d,e
Schumpeter Mark II	Level 5: Early R&D	300	a,b,c,d,e		0.045	a,b,c,d,e	0.045			a,b					a	a,b,c,d,e
					0.032	a,b,c,e	0.032									a,b,c,e
	Level 6: Mature R&D				0.028	a,b,e	0.028									a,b, e
					0.022	a	0.022									a
		INCREASING WAFER SIZE		SLOWING DOWN OF MOORE'S LAW												
		Continued Maximization		Continued Miniaturization			Continued Miniaturization				Advanced Integration					
		450mm	a,e	<22nm			<22nm				CoWoS (2.5D Packaging)				a,e	
											3D Packaging					

Source: Gartner (2012) and company official webpages.

M1 = MEMS; M2 = MCU (Embedded Flash); R = RF CMOS; A = Analog; B = BCD - Power IC; C = CMOS Image Sensor; D1 = High Voltage Driver; D2 = Embedded DRAM; L = Logic; .a = TSMC; b = UMC; c = GlobalFoundries; d = SMIC; e = Samsung; f = Silterra.

4.1 Process technology

Except the Malaysian owned pure-play foundry, it was found that the other five firms have managed to 'transit' to Schumpeter Mark II (creative accumulation) activities. The world four largest pure-play foundries – TSMC, UMC, Globalfoundries and SMIC as well as Korean Samsung have arrived at level 5 (early R&D stage) since their wafer manufacturing size has been migrated to 300mm, the biggest wafer diameter of the industry as of 2011. TSMC, Globalfoundries and Samsung have managed to reach level 6 (mature R&D stage) by participating in a joint development called the Global 450 Consortium which also includes IBM and Intel committing jointly to a $4.4B investment in the state of New York. The purpose of this consortium is to develop the technology of next generation wafer size at 450mm (New York State, 2011). SMIC and Silterra remain at level 4 (Schumpeter Mark I) not being able to migrate to 300mm which is more cost effective.

As for the process node miniaturization, thus far TSMC, UMC and Samsung foundry have managed to reach level 6 by fabricating at 28nm technology node. According to Gartner (2012b), only TSMC has officially announced two fabs (phase 6 of fab 12 and fab 16) which will be manufacturing at 22nm technology node by 2015. The minimum linewidth Globalfoundries is manufacturing is 32nm whereas SMIC managed to produce only at 45nm which leaves the two firms staying at level 5 (Figure 1 in appendix shows the miniaturization of technology nodes by the four largest pure-play foundries from year 2000-2010). It is important to note that in semiconductor DRAM industry, Samsung is the world leader and the firm has already arrived at 22nm. However, the miniaturization of memory chips is ahead of logic as it costs much less than a processor (logic chips). It is a series of simple and repeated structures which is not as complex as logic miniaturization since logic miniaturization requires making a single chip with several millions of individually-located transistors (PCTech Guide, 2011). In this case, Silterra is again classified as Schumpeter Mark I, being trapped at level 3 and manufactures at 0.13μm (Gartner, 2012b).

4.2 Product technology

As Table 2 shows, except Silterra Malaysia which has not been able to break the mold, all firms have transited to Schumpeter Mark II activities. TSMC, UMC and Samsung managed to conduct mature R&D (level 6) by producing logic ICs at 28nm. As the results shown in the proposed typology, TSMC not only leads in the race of miniaturization, the firm is also the most active and advanced in its More than Moore's strategy by innovating horizontally all the

product categories. Although not as aggressive as TSMC, Globalfoundries and SMIC are operating at level 5 by producing products at 45nm and 32nm. Table 2 also shows that the technology trajectory of Silterra Malaysia is again truncated at Schumpeter Mark I activities. Since Silterra does not have accumulation of financial resources as the rest of the firms and is not able to transit to Schumpeter Mark II, the firm's innovative activities are constrained and it can only retreat to horizontal expansion of product features, which means incremental innovations on products at the existing technology nodes and machineries.

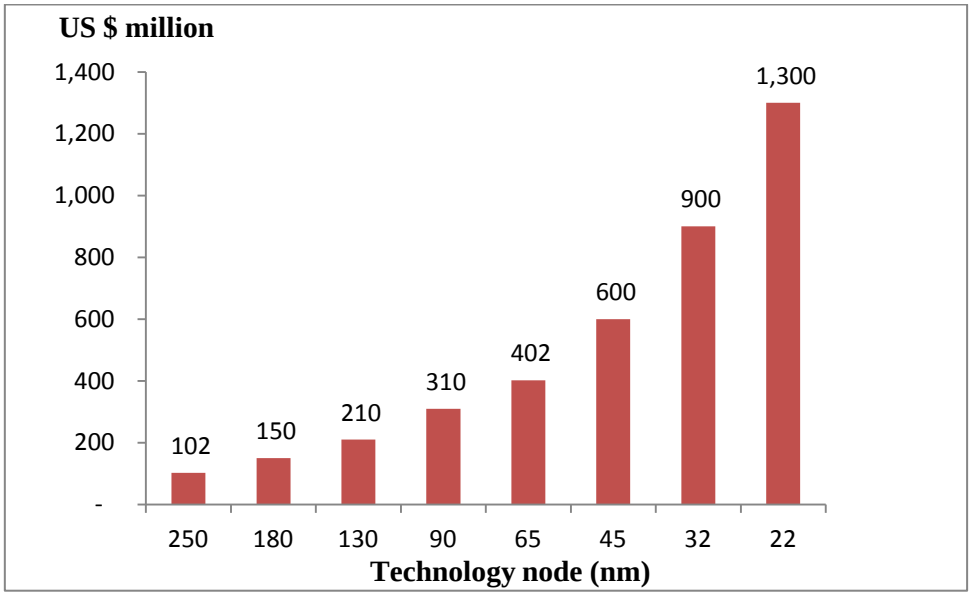
As Moore's Law slows down, firms which are able to conduct frontier R&D to create new advanced products are also categorized at level 6. In the foundry industry, the largest player – TSMC has been deploying lumpy investment into the R&D of CoWoS since 2007. This development allows the firm to do advanced forward integration by penetrating into the world of packaging. TSMC is able to offer a new line of services to its customers and such advanced technology level is not achievable even by the most advanced semiconductor packaging and assembly (SPA) firm in the industry. Thus far other industry key players like Intel and Samsung have not disclosed any detail on their schedules and roadmaps for CoWoS development (Lu et al., 2012a).

4.3 Discussion

Migration to a bigger wafer manufacturing size requires lumpy investments which require firms to pursue Schumpeter Mark II (creative accumulation) strategy. While foundries like SMIC and Silterra were trying to expand the lifetime of their existing fab and facilities to avoid high capital expenditure given their limited financial resources, the largest foundry - TSMC were continuously increasing the number of fabs and expanding its production capacity (Figure 2 in appendix shows the capacity mix of wafer size by the four largest pure-play foundries). By the end of 2011, TSMC owned a total of 19 wafer fabs, of which 9 of these wafer fabs' facilities were catered for advanced 300mm wafer manufacturing with minimum linewidth of 0.045μm or smaller (Vajpayee and Dhasmana, 2011). By 2010, 47% of the industry's capital spending in 2010 was attributed to TSMC, followed by GlobalFoundries (22%), UMC (approximately 12%), Samsung foundry (approximately 8%) and SMIC (approximately 4%) (Vajpayee and Dhasmana, 2011). It is apparent that these five foundries dominate the entire industry's capital spending by nearly 93% and they are also the only five in the industry which have managed to arrive at level 5 and level 6 in the technological typology.

Firms also require high level of R&D capabilities as well as strong financial resources (creative accumulation) to keep up with Moore's Law. The process development cost for more advanced technology nodes increases exponentially (see Figure 1). According to CLSA Research (2011), the cost of developing 22nm technology node is US$ 1.3 billion. The costs for the largest foundry, TSMC, to move to the 28nm node were twice that of the 65nm node. However, the largest foundry constantly invests heavily in R&D and the firm was the first in the industry to build massive capacity to produce at 28nm, 40nm and 60nm nodes. As of 2010, TSMC's R&D expenditure was US$ 728million, followed by UMC (US$ 242million), Globalfoundries (US$ 207million) and SMIC (US$ 181million) (CLSA Research, 2011). The R&D expenditure for the Schumpeter Mark I firm - Silterra in 2010 was approximately US$ 27million.

Figure 1: Process development cost for various technology nodes



Source: CLSA Research (2011).

The findings in this paper show that, in the semiconductor foundry industry, firm-level technological trajectory is indeed influenced by Schumpeterian patterns of innovation. However, there is no clear distinction between the level of focus given to process innovation and product innovation throughout the firms' life cycle. In fact, the relationship between process and product innovation is very much linked to the firms' Schumpeterian characteristics (creative destruction or creative accumulation). Foundries which are not able to transit to Schumpeter Mark II tend to limit their innovative activities on horizontal product technology development at the existing process nodes ('More than Moore' strategy), which are already considered obsolete for firms in Schumpeter Mark II.

Table 3: Top 20 semiconductor foundries (millions of U.S. dollars)

2009 Rank	2010 Rank	Company	2009 Revenue	2010 Revenue	2010 Share (%)
1	1	TSMC	8,997	13,332	47.1
2	2	UMC	2,730	3,824	13.5
3	3	Globalfoundries*	2,643	3,520	12.4
4	4	SMIC	1,070	1,554	5.5
7	5	Dongbu HiTek	370	512	1.8
8	6	TowerJazz	298	509	1.8
6	7	Vanguard International	381	505	1.8
5	8	IBM Microelectronics	383	500	1.8
10	9	MagnaChip	265	410	1.4
9	10	Samsung	290	390	1.4
14	11	HHNEC	207	370	1.3
12	12	X-Fab	211	317	1.1
11	13	Fujitsu Semiconductor	222	275	1
18	14	Grace Semiconductor	150	250	0.9
17	15	CSMC Technologies	151	225	0.8
15	16	HeJian Technology	175	212	0.7
16	17	Silterra	160	180	0.6
19	18	Rohm	141	174	0.6
20	19	Powerchip Technology	140	149	0.5
22	20	Phenitec Semiconductor	110	148	0.5
		Others	1,047	949	3.4
		Total Market	20,141	28,305	100

*2009 revenue shown is the combined revenue of Chartered Semiconductor ($1,542 million) and Globalfoundries ($1,101million).

Source: Gartner (2011).

Furthermore, Utterback and Abernathy's (1975) dynamic model of innovation does not apply specifically to even the foundry leaders. The semiconductor foundry industry requires the firms to develop their process and product technology almost concurrently throughout their technological trajectory. In order to lead the industry, the foundries race incessantly in the miniaturization of process nodes. Meanwhile, these firms require lumpy investments to migrate to bigger wafer manufacturing size by building new fabs and upgrading capacity or facilities with the objective to minimize cost. At the same time, even the largest foundry (TSMC) constantly develops its product technology features at all existing process nodes (see Table 2). Therefore, as Utterback and Abernathy (1975) had argued, there is indeed interdependency between process and product innovation. However, in the foundry industry, the process and product innovation as well as cost minimization progress parallelly and are

equally important for a firm to arrive at the frontier of knowledge depth (Schumpeter Mark II) and lead the industry regardless the stage of the firm in the life cycle.

Table 3 shows the ranking of the foundry industry as of 2010 according to revenues and market share. TSMC leads the industry by owning 47% of the market share, followed by UMC which owns 13.5% market share. Globalfoundries follows closely at number 3 with 12.4% market share, whereas SMIC charts number 4 by having 5.5% of the market share. Samsung foundry is ranked number 10 in year 2010 given its revenue as high as US $ 390 million. Malaysian Silterra is listed at number 17 in the worldwide ranking of top 20 foundries (Gartner, 2011).

5. Conclusion

The proposed typology of technological taxonomy and trajectory in this paper is an attempt to distinguish firm-level depth of knowledge by Schumpeter Mark I and Schumpeter Mark II, at the same time incorporating the dynamics of the foundry industry. This paper also argues that there is no specific trend of process and product innovation among foundries across their life cycle; thus Utterback and Abernathy's (1975) model of innovation does not apply specifically to the foundry industry. In the foundry industry, process and product innovation as well as cost minimization are equally important to all firms throughout their life cycle and the level of these developments (knowledge depth) depends very much on the Schumpeterian patterns of innovation.

The findings in this paper corroborate with the evolutionary argument that technological upgrading is industry specific and so studies conducted on technological development should deal with the uniqueness of each industry. Firms' technological trajectory and the interdependency between their process and product innovation depends very much on the technological regime involved as the technological regime will define the industry's Schumpeterian patterns of innovation.

It is essential for future research on the foundries' technology typology to incorporate other aspects which may be important, such as advanced backward integration, manufacturing system, as well as chip design capabilities. Understanding industry specificities is critical to identify specific drivers of firm-level technological upgrading. Moreover, it enhances understanding of industrial dynamics which is essential to formulate relevant industrial policies and to appropriate institutional change.

References

Abernathy, W. and Utterback, J., 1978. Patterns of industrial innovation. *Technology Review*, June/ July, pp.39-48.

Bell, M., 2006. Time and technological learning in industrializing countries: how long does it take? How fast is it moving (if at all)? *International Journal of Technology Management*, 36 (1-3), pp.25–39.

Breschi, S., Malerba, F. and Orsenigo, L., 2000. Technological regimes and Shumpeterian patterns of innovation. *Economic Journal*, 110(463), pp.388-410.

Brown, C. and Linden, G., 2009. C*hips and change: how crisis reshapes the semiconductor industry*. Cambridge: The Massachusetts Institute of Technology (MIT) Press.

CLSA Research, 2011. Available through: CLSA Asia-Pacific Markets research database. [Accessed 13 June 2012].

Credit Suisse Research, 2011. Available through: Foundry database.[Accessed 15 June 2012].

Dosi, G., 1982. Technological paradigms and technological trajectories. *Research Policy*, 11, pp.147-162.

Dubash, M., 2005. Moore's Law is dead, says Gordon Moore, *Techworld*, [online]13 April. Available at:<http://news.techworld.com/operating-systems/3477/moores-law-is-dead-says-gordon-moore/>[Accessed 3 May 2012].

Ettlie, J., 1995. Product-process development integration in manufacturing. *Management Science,* 41(7), pp.1224–1237.

Figueiredo, P., 2010. Discontinuous innovation capability accumulation in latecomer natural resource-processing firms. *Technological Forecasting and Social Change*, 77(2010), pp.1090-1108.

Gartner, 2011. Market share analysis: Semiconductor foundry, worldwide, 2010. Gartner Research report. April 2011.

Gartner, 2012a. Gartner says semiconductor foundry market grew 5.1 percent in 2011 to reach $29.8 Billion. *Gartner,* 30 March.

Gartner, 2012b. Fab database: worldwide, second quarter 2012 update. Gartner Research.

George-Cosh, D., 2010. ATIC increases stake in Globalfoundries. *The National*,29 December.

Gerschenkron, A., 1962. *Economic backwardness in historical perspective*. Harvard: The Belknap Press of Harvard University Press.

Kim, L., 1980. Stages of development of industrial technology in a developing country: A model. *Research Policy,* 9(1980), pp.254-277.

Kim, L., 1997. *From imitation to innovation*. Cambridge: Harvard Business School Press.

Kim, L., 1999. Building technological capability for industrialization: analytical frameworks and Korea's experience. *Industrial and Corporate Change*, 8(1), pp.111-136.

Lall, S., 1992. Technological capabilities and industrialisation. *World Development*, 20(2), pp.165-186.

LaPedus, M., 2007. Industry socked by next-gen litho woes. *EE Times*, 5 March.

Lee, K. and Lim, C., 2001. Technological regimes, catching-up and leapfrogging: Findings from the Korean industries. *Research Policy*, 30(2001), pp.459-483.

Lee, K., 2005. Making a technological catch-up: barriers and opportunities. *Asian Journal of Technology Innovation*, 13(2), pp.97–131.

Lu, B., Chen, H. and Chen, E., 2012a. TSMC. Research Report. *CLSA Asia-Pacific Markets*, March 2012.

Lu, B., Chen, H. and Chen, E., 2012b. Taiwan semiconductor: sector outlook. Research Report. *CLSA Asia-Pacific Markets*, March 2012.

Malerba, F. and Orsenigo, L., 1996. Schumpeterian patterns of innovation are technology-specific. *Research Policy*, 25(1996), pp.451-478.

Nelson, R., and Winter, S., 1982. *An evolutionary theory of economic change*. Cambridge: Harvard University Press.

Nelson, R., 2008a. What enables rapid economic progress: what are the needed institutions? *Research Policy*, 37(1), pp.1-11.

Nelson, R., 2008b. Economic development from the perspective of evolutionary economic theory. *Oxford Development Studies*, 36(1), pp. 9-21.

New York State, 2011. Governor Cuomo announces $4.4 billion investment by International Technology Group led by Intel and IBM to develop next generation computer chip technology in New York. *New York State*, 27 September.

Pavitt, K., 1984. Sectoral patterns of technical change: towards a taxonomy and a theory. *Research Policy*, 13(1984), pp.343-373.

PCTech Guide, 2011. DRAM – Dynamic Random Access Memory, *PCTech Guide*, [online]. Available at:< http://www.pctechguide.com/computer-memory/dram-dynamic-random-access-memory>[Accessed 12May 2012].

Perez, C., 1988. New technologies and development. In C. Freeman and B. Lundvall (Ed.), *Small countries facing the technological revolution* (pp.85-97). London: Pinter Publishers.

Perry, T., 2011. Foundry father Morris Chang pioneered the $28 billion semiconductor foundry industry, kicking off a revolution in the business of chips. IEEE medal of

honor, *IEEE Spectrum*: pp.46-50.

Rasiah, R., 1994. Flexible production systems and local machine tool subcontracting: electronics component transnationals in Malaysia. *Cambridge Journal of Economics*, 18(3), pp.279-298.

Rasiah, R. 1996. Institutions and innovations: moving towards the technology frontier in the electronics industry in Malaysia. *Industry and Innovation*, 3(2), pp.79-102.

Rasiah, R., 2004. Technological intensities in East and Southeast Asian electronics firms: does network strength matter? *Oxford Development Studies*, 32(3), pp.433-455.

Rasiah, R., 2010. Are electronics firms in Malaysia catching up in the technology ladder? *Journal of Asia Pacific Economy*, 15(3), pp.301-319.

Rasiah, R., 2011. Ownership and technological capabilities: evidence from automotive firms in Brazil, India and South Africa. *International Journal of Institutions and Economies*, 3(2), pp.203-234.

Rasiah, R., Kong, X.-X., Lin, Y. and Song, J., 2012. Variations in the catch up experience in the semiconductor industry in China, Korea, Malaysia and Taiwan. In F. Malerba and R. Nelson, ed. *Economic development as a learning process: Differences across sectoral systems.* Cheltenham: Edward Elgar.

Rasiah, R. and Vinanchiarachi, J., 2012. Institutional support and technological upgrading: evidence from dynamic clusters in Latin America and Asia. Faculty of Economics and Administration, University of Malaya. (mimeo)

Schumpeter, J., 1912. *The theory of economic development*. Cambridge, Mass: Harvard University Press.

Schumpeter, J., 1934. *The theory of economic development: an inquiry into profits, capital, credit, interest and the business cycle*. London: Oxford University Press.

Schumpeter, J., 1943. *Capitalism, socialism and democracy*. London: Allen & Unwin.

Utterback, J. and Abernathy, W., 1975. A dynamic model of process and product innovation. *The International Journal of Management Science*, 3(6), pp.639-656.

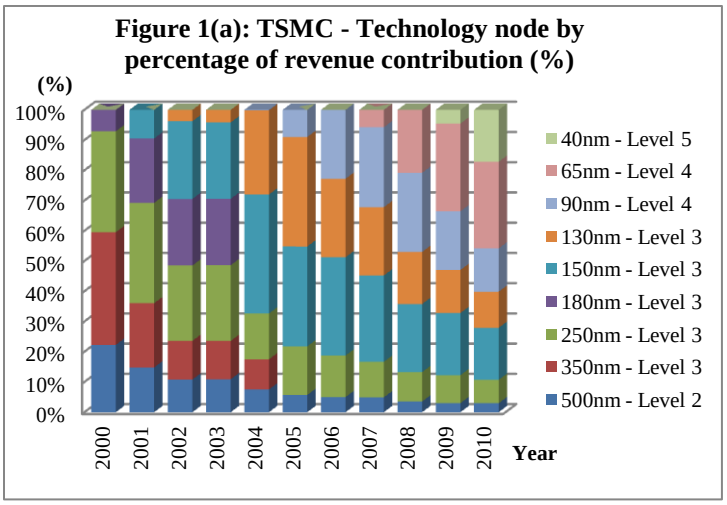
Vajpayee, B. and Dhasmana, V., 2011. Semicon foundries: sector outlook. Research Report. *CLSA Asia-Pacific Markets*, January 2011.

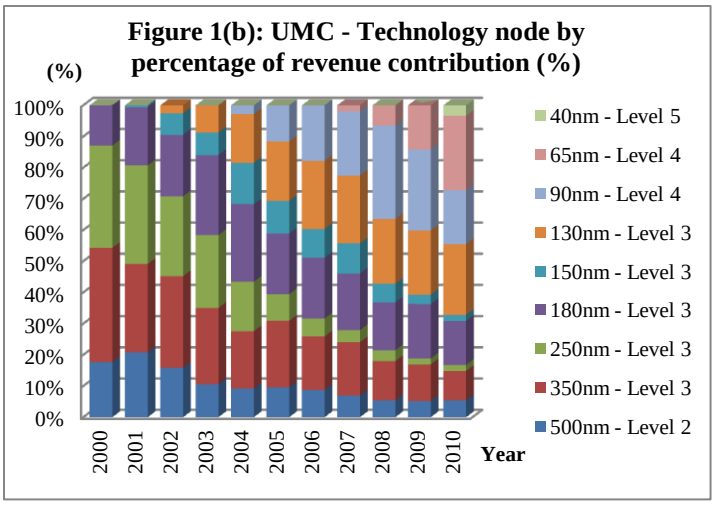
Winter, S., 1984. Shumpeterian competition in alternative technological regimes. *Journal of Economic Behavior & Organization*, 5, pp.287-320.

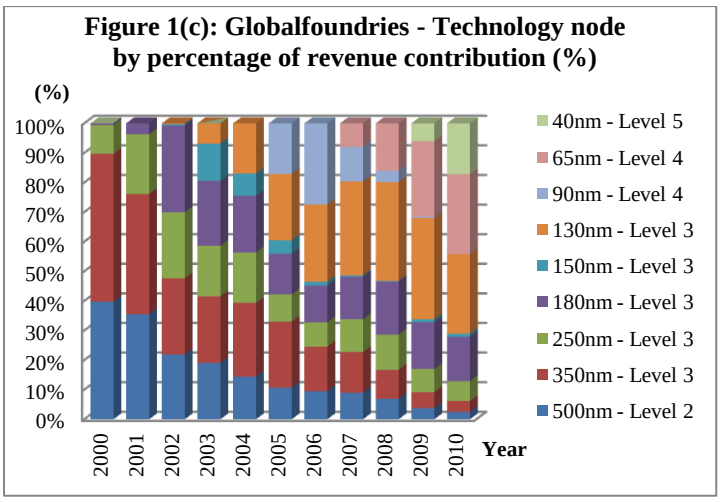
Winter, S., 1987. Knowledge and competence as strategic assets. In: D. J. Teece, ed. *The competitive challenge: strategies for industrial innovation and renewal*. Cambridge Mass: Ballinger, pp.159-184.

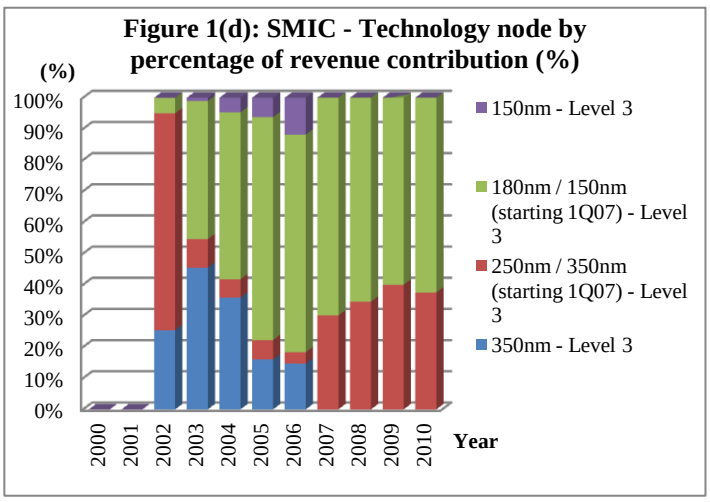
Appendix

Figure 1: Miniaturization of technology nodes by four largest pure-play foundries



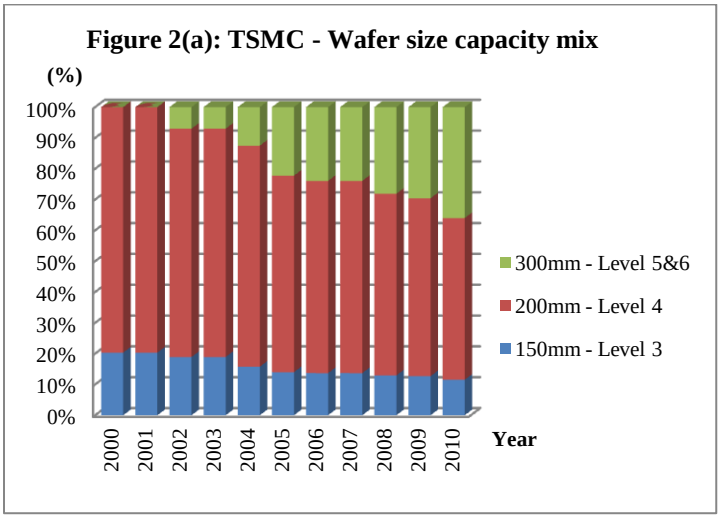


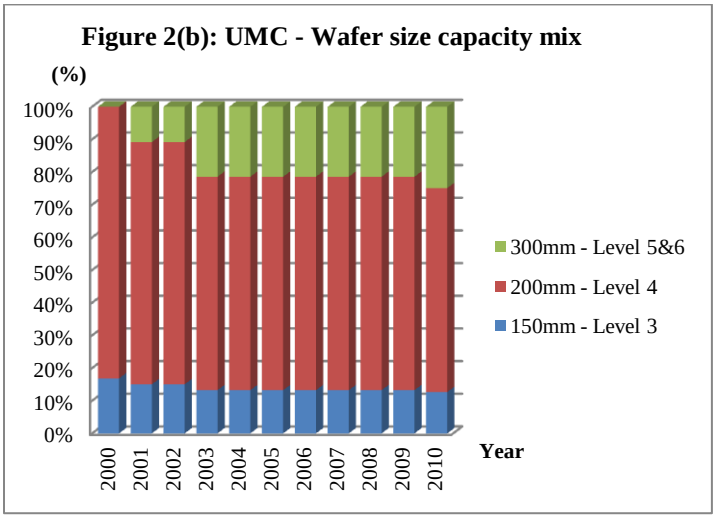


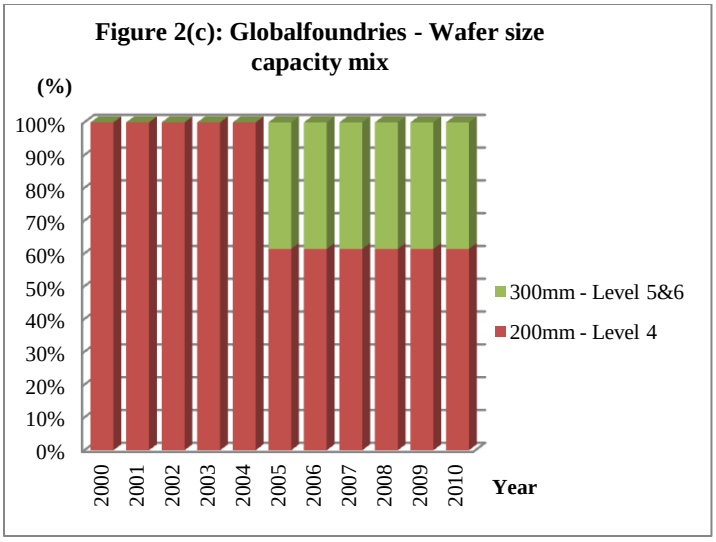


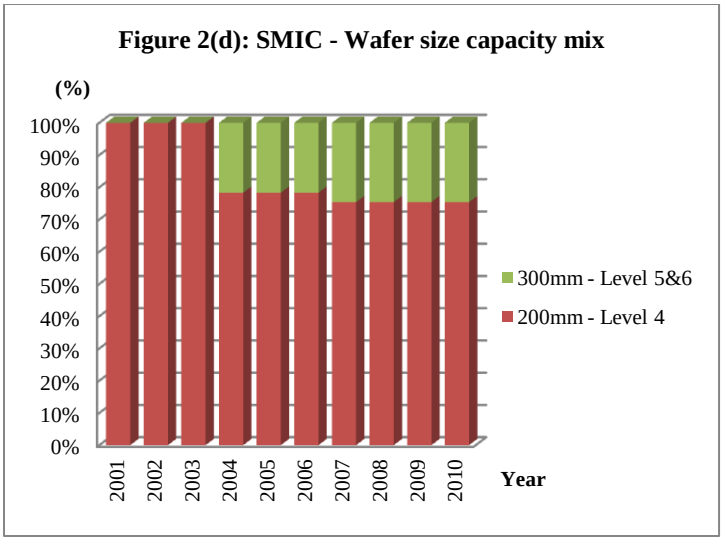
Source: Credit Suisse Research (2011) and Gartner (2012).

Figure 2: Wafer size capacity mix of four largest pure-play foundries









Source: Credit Suisse Research (2011) and Gartner (2012).